What is HyperTransport?

HyperTransport technology is an advanced, royalty-free, high-speed link for "in-the-box" IC (Integrated Circuit) connections. It offers very high bandwidth and flexible scalability in terms of both speed and bus width; for instance, specification 1.x already enables chips to communicate with each other up to 48 times faster than with existing PCI technology while maintaining complete compatibility with PCI technology (see Figure 1). The most current specification 2.0, which adds the three additional new speeds 2.0 GT/s (GigaTransfers/second), 2.4 GT/s and 2.8 GT/s, to the HyperTransport technology specification, further boosts this to 18 Gigabyte/second, 19.2 Gigabyte/second and 22.4 Gigabyte/second aggregate bandwidth, respectively.

![HyperTransport Technology Key Features](image)

Although HyperTransport technology was originated by AMD and its partners, HyperTransport-enabled applications are not limited to PC processor – chipset connections (Figure 2), but include many diverse, high-volume applications:

- Consumer: e.g. game consoles
- Computing: e.g. desktop PCs, portable servers
- Networking: e.g. network equipment and customer premise equipment (CPE)
- Embedded: e.g. printers

![HyperTransport Architecture](image)

The success of HyperTransport is a result of its ability to deliver fast, scalable chip-to-chip bandwidth using a protocol that is relatively inexpensive to implement and is totally PCI software transparent. It has become the first among the newly emerging 3rd generation I/O standards to be adopted and implemented in large volume. Indeed, a number of high-volume HyperTransport applications mainly running at 800 Mbps data rate are already available on the market: the most prominent example today is Microsoft’s® Xbox® using HyperTransport as a 800 Mbps connection between the Nvidia “Graphics Processor Unit” (GPU) – a Northbridge chipset device with integrated graphics – and the “Media and Communications Processor” (MCP) Southbridge chipset (see Figure 3).

The major step towards 1.6 Gbps data rate has been made with the introduction of AMD’s K8 processor family (Figure 2) in 2003, for which all major chipset companies (except

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1 Data rates currently range from 400 Mbps up to 2.8 Gbps, and bus widths from 2 bits up to 32 bits.

2 See the box “The I/O Technology Battle” on page 5.

3 Microsoft is a U.S. trademark of Microsoft Corporation.

4 Microsoft Xbox is a product of Microsoft Corporation.
The physical layer:

Conceptually, the architecture of the HyperTransport I/O link can be mapped into five different layers, whose structure is similar to the Open System Interconnection (OSI) reference model. The physical layer defines the physical and electrical characteristics of the protocol. This layer interfaces to the physical world and includes the data, clock, and control lines. The HyperTransport link actually consists of two independent source-synchronously clocked uni-directional sets of wires, where each set of wires includes CAD (command, addresses, data), CLK (clock), and CTL (control) pins.

The high-speed data rates, ranging from 400 million transfers per second (Mbps) up to a current maximum of 2.8 Gbps, are achieved by employing a type of low-voltage differential signaling (LVDS) with on-die differential termination. CAD signals traveling on a HyperTransport link utilize a double data rate technique, i.e. transfers take place on both the rising and falling edges of the clock signal.

In differential signaling, the true signal is sampled by the receiving device while using the complement signal as a voltage reference. A logic 1 occurs when the true signal is greater than the complement, whereas a logic 0 occurs when the true signal is less than the complement. The signal swing ranges from 300 mV to 900 mV and swings around 600 mV (common mode voltage). The termination of each signal is done at both the source and the receiver. There are no external motherboard pull-ups or pull-downs. This is illustrated in Figure 5.

HyperTransport Testing Challenges and the Agilent 93000 Solution

Up to data rates of 800 Mbps, the Agilent 93000 SDC Series P-Models can be safely employed for testing HyperTransport devices. However, for higher speeds, new
phenomena, which mainly originate from the differential and source-synchronous nature of HyperTransport signaling, get more pronounced; thus, new test methodologies and new test equipment are required to cope with these specific test problems. For addressing these challenges, Agilent has extended the well-established 93000 SOC platform with the high-speed NP-models: The NP1700 and NP2500 pin electronic cards (Figure 6) allow up to 256 high-speed, true differential drive/receive pairs with existing 93000 digital and analog cards.

The Agilent 93000 SOC Series with its NP1700-Model for data rates up to 1.7 Gbps, and NP2500 for data rates up to 2.5 Gbps, are exactly targeted at this speed challenge. In addition, the NP1700-Model can be simply upgraded by software to the NP2500-Model, and both models can even deliver signals as fast as 3.2Gbps in an extended speed mode.

Low Voltage Differential Signaling
Since HyperTransport employs low-voltage differential signaling, it is of great advantage when the ATE pin electronics supports this signaling to make sure that the test environment actually matches the application. For this reason, the NP-Models feature a native differential driver and receiver architecture: whereas the driver is implemented as a current switch for ensuring highest symmetry of the differential signal, the receiver offers a 100Ω cross-termination mode.

Source Synchronous Operation
HyperTransport utilizes a source synchronous timing scheme: along with the data, a clock signal is forwarded, which originates from the same timing source. For high data rates and devices having many switching transistors at the same time (e.g. microprocessor units), it is necessary to operate tests also in a source synchronous fashion; otherwise, timing margins are significantly reduced. In contrast to conventional ATE hardware, which only operates in a tester synchronous mode (i.e. with a fixed timing reference), the NP-Models also feature a built-in source synchronous operation mode (Figure 7). The operation mode of the NP-receivers from source synchronous to tester synchronous can be easily switched from one test to the other without any hardware modifications.

Jitter measurements
For high-speed interfaces such as HyperTransport, accurate jitter measurements are of particular importance, since excessive jitter potentially belongs to the device’s dominating failing mechanisms. In order to be able to do accurate jitter measurements, the ATE system must not add additional jitter. The NP-Models use therefore a retiming architecture to ensure lowest intrinsic system jitter.

In the following, we discuss the most demanding HyperTransport-specific test challenges in some detail:

High-Speed Data Rate
Since HyperTransport operates at data rates up to 2.8 Gbps, at-speed functional tests require ultra fast ATE pin electronics, which accommodate this speed range. Moreover, especially for characterization tests, it is desirable to go beyond the specified speed by at least 5%.

Figure 6: Agilent NP-Model pin electronics card (right), which hosts 4 differential drivers and 4 differential receivers, resides in the Agilent 93000 SOC Series testhead (left).

Key characteristics of Agilent 93000 NP-Models

- Delivers cleanest signals as fast as 3.2 Gbps guaranteed by true differential drivers combined with lowest-jitter re-timing architecture
- Highest receive bandwidth > 3 GHz for high-accuracy parametric measurements
- Ultra-fast jitter measurement capability; 60 ports in < 1 sec
- Built-in at-speed scope functionality
- Native source synchronous support
- Allows complete HyperTransport characterization by exclusively using pin electronic cards, i.e. no need to use any additional external instruments

Also, a center-tap termination mode for other applications is provided.
When using de-emphasis, in a row of consecutive bits of the same logical level, only the first bit is driven at nominal differential swing. All consecutive bits in this row are attenuated according to the de-ratio parameter specified for HyperTransport. After sending such a signal through a connection generating droop, the levels of all of the bits are quite equal. Since droop is caused by bandwidth limitations on the PCB connections, it is of utmost importance that the measurement resources used to verify this parameter offer sufficient bandwidth. Otherwise, the bandwidth limitation of the measurement resource itself would cause the de-emphasis effect to vanish. With their bandwidth of >3GHz, NP2500 receivers are perfectly capable of testing de-emphasis waveforms generated by HyperTransport as shown in Figure 8. It has to be noted, that de-emphasis is a pure DUT driver specification. This means that the ATE has to be able to test this parameter, but not to generate de-emphasized waveforms.

Figure 8: A low swing 2.4Gbps waveform with de-emphasis measured by Agilent 93000 SOC Series NP2500 Model.

Impedance (DC) measurements
HyperTransport uses on-die termination for minimizing signal reflections and ringing. Hence, input and output impedance tests are necessary for which the ATE-system needs full DC measurement capabilities. The NP-Models therefore also support single-ended measurements for up to 1.25 Gbps on each line of the differential pair, including complete DC test capabilities via per-pin PMU.
The transition from characterization to production

It is important to note that all of the above-described measurements can be done solely with the pin electronics of the 93000 NP-Models without the necessity to use any external instruments. This is especially important for a smooth and rapid transition of a device from the characterization to the production and finally the high-volume manufacturing phase, since this guarantees the least test correlation effort.

HyperTransport Consortium & Outlook

HyperTransport was originally developed by AMD and its partners, and AMD still supports the further development of this technology as a promoter member in the HyperTransport industry consortium. Unlike many proprietary technologies that were presented as “open standards,” HyperTransport Technology has achieved remarkable industry success because it was quickly transferred from AMD and its partners to a general industry consortium that defined a clear specification and opened the technical development to member companies. In addition, HyperTransport technology is provided royalty-free with just an administrative cost for the license itself. The consortium manages and controls the HyperTransport technology specification, promotes the proliferation of HyperTransport technology in the industry, and assists the consortium member companies in pursuing their business interests. More information on the consortium can be found on the following website: http://www.hypertransport.org/

As one of the 50+ consortium members, Agilent is actively engaged in numerous consortium activities. One particular example is the consortium’s compatibility program. This program ensures that a device is compatible with the HyperTransport specification by providing testing checklists and other technical recommendations. Devices which have participated in the program, will be listed on the compatibility program public website.

Although the HyperTransport technology already generated a wide product eco-system, ranging from silicon, software, IP, and tool companies, it will be further developed. The next major step with specification 2.0 is targeted for 3rd Q. 2003, and is expected to provide double speed operation.

The I/O Technology Battle

With the recent explosion of processor clock rates, I/O buses have become the bottleneck in boosting data throughput in compute and communication appliances. Though the interface standards-war between the proposed I/O technologies such as HyperTransport, RapidIO, Serial-ATA, InfiniBand, and PCI Express (to mention the most discussed ones) has not yet been fully settled, it seems that HyperTransport has already successfully established itself. Table 1 gives a quick overview of emerging I/O technologies whose primary focus are compute-intensive applications.

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8 Other promoter members are Alliance Semiconductor, Apple Computer, Broadcom Corporation, Cisco Systems, NVIDIA, PMC-Sierra, Sun MicrosystemsTM, and Transmeta. Sun Microsystems is a registered trademark of Sun Microsystems, Inc. in the U.S. and other countries.

9 Agilent, for example, has provided a white paper entitled “Characterization of HyperTransport Interfaces on Agilent 93000 SCC Series” which is available on the consortium’s (members-only) website.
<table>
<thead>
<tr>
<th>Feature</th>
<th>HyperTransport</th>
<th>RapidIO</th>
<th>Serial ATA</th>
<th>InfiniBand</th>
<th>PCI Express</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current (max.) data rate</td>
<td>400 Mbps up to 2.8 Gbps</td>
<td>Parallel: up to 2 Gbps, Serial: up to 3.125 Gbps</td>
<td>1.5 Gbps</td>
<td>2.5 Gbps</td>
<td>2.6 Gbps</td>
</tr>
<tr>
<td>Technology characteristics</td>
<td>Parallel source synchronous</td>
<td>Parallel source sync + serial embedded clock</td>
<td>Serial embedded clock</td>
<td>Serial embedded clock</td>
<td>Serial embedded clock</td>
</tr>
<tr>
<td>Target Applications</td>
<td>Universal &quot;in-the-box&quot; chip-to-chip</td>
<td>Chip-to-chip + board-to-board via backplane, primarily for networking and communications</td>
<td>&quot;In-the-box&quot; physical storage interface</td>
<td>Server clusters + data-center fabric</td>
<td>&quot;In-the-box&quot; chip-to-chip, board-to-board, as well as &quot;out-of-box&quot; general purpose I/O for computation and communication</td>
</tr>
<tr>
<td>Maximum trace length</td>
<td>Inches</td>
<td>Inches</td>
<td>Inches - meters</td>
<td>km</td>
<td>Inches - meters</td>
</tr>
<tr>
<td>Transport media</td>
<td>PCB only</td>
<td>PCB: fiber, copper</td>
<td>PCB + cables</td>
<td>PCB, fiber, copper</td>
<td>PCB + cables</td>
</tr>
<tr>
<td>Scalability</td>
<td>Yes, both data and bus width</td>
<td>Yes</td>
<td>No</td>
<td>Yes, only bus width</td>
<td>Yes, only bus width</td>
</tr>
</tbody>
</table>

Table 1: Comparison-primer of different high-speed I/O standards.