HyperTransport™ High Node Count
System-Wide Resource-Sharing

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Industry Snapshot

Data Centers, Cloud, HPC Drive Technology

Squeeze is on Industry for:
• Minimized Power Footprint
• Optimized Resource Usage
• Lowest TCO

and of course…
• Peak Performance

Simply Put: *All of Everything for Less*
1st Step - Technology-Level Virtualization (1.0)

- Software Virtualization
  - Hypervisor
- CPU Virtualization
  - AMD-V™
  - Rapid Virtualization Indexing
- I/O Virtualization
  - AMD-Vi™ - Chipset-Level

Not Bad for a Start
2nd Step - System-Level Virtualization (1.1)

- Consolidation
  - Greater Number of Virtualized CPU Sockets per Server Chassis (4-8)
    - Lower I/O Redundancy, Lower Power, Lower Cost

- Convergence
  - Storage Interconnect Protocol Encapsulated into 10G Ethernet (FCoE), InfiniBand (FCoIB)
    - Interconnect Medium Sharing, Lower System Cost

Another Good Step Forward

But Hardly Fulfilling All Market Expectations

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Ultimate Objective: **System-Wide Virtualization** (2.0)

- Global Resource Sharing **Without Node Scalability Limitations**
  - Eliminates Resources Over-Provisioning
- Function-Specific Nodes (Computing, Acceleration, Storage, …)
  - Shed In-System Hardware Redundancy
- Node Granularity and Modularity
  - Simplify Product Configuration, Stocking, Application-Specific Tailoring, Field Upgrading and Maintenance
- Maximized Power Efficiency and Cost Containment
System-Wide Virtualization 2.0
Transcends Single Technology Ability to Fulfill Global Objective

Each Technology has Partial/No Influence Over Others
- e.g. System Interconnects (10GE, IB) Do Not Control/Affect Processor Performance
- Processors Do Not Control/Affect Cluster Resource-Sharing and Scalability
- Servers Virtualize their Own Internal Resources Only
- Efficient CPU Cache Coherency is Limited in Node Scalability
Has Influence Over Collective Cluster Technologies
It is the Vehicle to Resource Partitioning and Sharing
It Directly Affects Cluster Performance

System-Wide Interconnect Technology
Key to Virtualization 2.0

Industry Snapshot (cont.)
Vision-Driven HyperTransport Evolution

From Chip-to-Chip
to System-Wide Interconnect Technology

Note 1: by end of 2003 – Source InStat
Note 2: by end of 2008 – Source InStat
Note 3: High Node Count Specification 1.0 - Accessible/Useable by Promoter and Contributor Members Only

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High Node Count Specification

Answers the Challenge of Addressing Exponential Number of Compute Cores and Nodes
High Node Count Specification (cont.)

Answers the Challenge of Addressing Exponential Number of Compute Cores and Nodes

Maximized Scalability

Performance-Optimized for Clusters of Any Size and Scale
Global Shared Memory
Physically Distributed Resource Sharing and Partitioning

System-Wide Resource Sharing

Localized Compute, Acceleration and Memory Resources Serve the Whole Cluster

Heterogeneous Resource Partitioning Optimizes TCO
High Node Count Specification (cont.)

Non-Coherent Cluster Interconnect Backbone
With Coherent Sub-Cluster Support

Leverages Existing Infrastructure

Bypasses Cache-Coherence Scalability Limitations via HNC System-Wide Addressing Scheme
High Node Count Specification (cont.)

HT Encapsulation Over InfiniBand and Ethernet

Latency Bottleneck of Message-Passing Protocol

HT Encapsulation Bypasses Message-Passing Software

Remove the Latency Overhead Penalty of Less Efficient Message-Passing Protocols

Leverages Existing Infrastructure With a Twist!
High Node Count Specification (cont.)

Heterogeneous Node Function Clustering
Maximum Modularity

Any Configuration of HT-Based CPU, Accelerator, Memory and Peripheral Nodes

System Flexibility  
Cost-Optimization  
Power-Optimization  

Minimized Over-Provisioning  
Optimized Resource Utilization
Wide Choice of Node Processors

HT-Based Coherent and Non-Coherent CPUs, Accelerators and Specialty Processors

Empowers System Manufacturers
Enables Nodes to be Application-Specific
Leverages Low-Power Processors
Achieves Optimum TCO
High Node Count Specification (cont.)

System-Wide **HT-Native** Interconnect Infrastructure

Further Eliminates the Hardware and Protocol Latency Overhead of 10GE and IB

Global Resource Sharing

Lowest Latency

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HT Connectors and Cables

In-System and System-Wide HNC Enablement

- Standardized HNC Enablement
- Vast System Modularity Latitude
  - For Systems and Subsystems
- HT 3.1 Performance
- Highly Compact
- HT-Specific Signal Allocation
  - Optimized Signal Integrity and Routing
- Modular
HT Node Connectors and Cables

Long-Haul HT / HNC Connectivity
Greatly Expanded System Modularity

**Vertical Mount and Right Angle Female Connectors**
- High Density 0.635mm Pitch
- Mate with Cable Connectors

**Universal Male Connector Cable**
- 32-AWG Twinax Cable
- Copper Shielding
- Smooth Insertion Loss Profile to 16 GHz
- Full HT3.1 Performance to 2m Length
HT Node Connectors and Cables (cont.)

Right Angle Connector Applications

- 6x 8-Bit / 3x 16-Bit HT Links Fit in Full-Height HTX/PCIe Board
  - Supports 3D Torus/Mesh HT NICs and Switches
- MB-to-MB and MB-to-Appliance HT Links
- High-Density Rack Switches and Blade Servers
Vertical Mount Connector Applications

- PCIe Slot Used Only for Power Feed and Mechanical Support
- CPU Socket Adapter Compatible with All MBs
- Excellent Signal Integrity
  No PCB Signal Degradation
HT Mezzanine Connectors

Answer to HNC Mezzanine Cards Modularity

- 2x 8-Bit or 1x 16-Bit HT Links in Single Connector Shell
- Signal Layout Optimized for Easy Escape Routing
- HT Signals, Power and 10 User-Available Pins
- Compact 56.6 x 5.6mm Footprint
- Low Profile - Choice of Stacking Heights
- Ruggedized
- Multi-Standard Certified
- Full Productions
- Second Sourced
HT Mezzanine Connectors (cont.)

Applications

• Modular In-System Functions and Interfaces
• High-Performance NICs
• Accelerator Modules
• Multiprocessor Modules
• Special Functions
**HT Mezzanine Connectors (cont.)**

**Applications (cont.)**

- CPU-to-Internal-Subsystem Direct HT Links
- Excellent Signal Integrity
  No PCB Signal Degradation
- PCIe Slot Used Only for Power Feed and Mechanical Support
- CPU Socket Adapter
  Compatible with All MBs