HyperTransport™

HTX™ Slot Connectors

Applications
**HTX Target Markets**

- Database Analytics
- Stock Trading Acceleration
- High-Traffic Web-Based Applications
- Transaction Servers
- Streaming Media Servers
- Storage Servers
- Server Clustering and SMP
- Financial Modeling
- Communications
- Content / Security Processing

Requiring Compute-Intensive Subsystems Featuring:
- Lowest Latency
- Multi-CPU Connections
- Advanced Power Management
HTX Applications

With its Unique Architectural and Performance Edge over General Purpose Interconnects, HTX is an Ideal Complement to PCI-Class Slot Connector Interfaces
HTX System Implementation

- Uses popular PCIe Connector
  - High-volume part, Low cost
- HT-defined Signals
- Reverse-Installed vs. PCIe Slots
  - Prevents Wrong Card Insertion

HTX Connector
HTX System Implementation (cont.)

- Vertical Mount
- Horizontal Mount via HTX Riser
HyperTransport™

HTX™ Slot Connectors

Features
HyperTransport *HTX*

- Lowest Latency, Highest Bandwidth
  Direct Connect Between CPU and Compute-Intensive Subsystems
- Removes Performance Bottlenecks in HPC Processing and Co-Processing
  - No Intermediate CPU-to-Subsystem Control Logic
- Reduces Overall Power Consumption
- Complements PCI-Class Interconnects
  - Co-Exists with PCI-X and PCIe Connectors in Same MB

**Features**

- 8-Bit and 16-Bit HyperTransport Link Support
- 800 MHz Max Clock Rate
- 6.4 GB/s Bandwidth (16-bit, Aggregate)
HyperTransport *HTX*

**Lowest Achievable Latency**

- **No Control Logic Latency Penalty**
  - CPU
  - HTX™ High-Perf Subsystem

- **Control Logic Latency Penalty**
  - CPU
  - Chipset
  - Peripheral

*Performance*

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HyperTransport HTX

Lowest Achievable Latency (cont.)

No 8B/10B Overhead Penalty

Setup/Hold Receiver (No SerDes)

Data

Clock

Data

Clock

20% 8B/10B Fixed Overhead Penalty

Data Recovery (SerDes)

Data

Ref. Clock

Data

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Lowest Achievable Latency (cont.)

Minimized Packet Overhead

12 Byte Overhead Penalty vs. HT

Performance
HyperTransport *HTX3*™

- >3x Bandwidth of Standard HTX
- Brings HT 3.0 Performance and Architectural Latitude to HTX Connector
- Triples HT Clock Rate While Preserving Signal Integrity
  - Leverages HT 3.0 Clock Recovery “Scrambling” and “Training” Features
- Adds Power Management Features
- Adds Link-Splitting Capability
  - Supports 2x CPU HT Links
### HTX - HTX3 Features Summary

<table>
<thead>
<tr>
<th>Feature</th>
<th>HTX</th>
<th>HTX3</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Clock Rate</td>
<td>800 MHz</td>
<td>2.6 GHz</td>
<td>12” Trace length</td>
</tr>
<tr>
<td>Max Bandwidth x Lane</td>
<td>1.6 GT/s</td>
<td>5.2 GT/s</td>
<td>Bi-directional</td>
</tr>
<tr>
<td>Max Bandwidth Aggregate</td>
<td>6.4 GB/s</td>
<td>20.8 GB/s</td>
<td>Bi-directional 16-Bit HT link</td>
</tr>
<tr>
<td>HT3 Link Splitting Support</td>
<td>NO</td>
<td>YES</td>
<td>HT link can be 1x 16-Bit or 2x 8-Bit for multi-CPU support</td>
</tr>
<tr>
<td>HT3 Extended Power Management</td>
<td>NO</td>
<td>YES</td>
<td>LDTREQ# Signal Added to participate in x86 power states</td>
</tr>
<tr>
<td>Extended FPGA Guidelines</td>
<td>NO</td>
<td>YES</td>
<td>Incorporated field-proven recommendations</td>
</tr>
<tr>
<td>Full Backward Compatibility</td>
<td>--</td>
<td>YES</td>
<td>Level shifters and signal allocation</td>
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</table>
HTX BIOS Support

Consortium-Defined and Standardized
HTX™ BIOS Specifications

Cross-Compatibility          Fast Time-to-Market