HyperTransport™ Technology

General Overview

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General Overview Coverage

- Compute-Intensive Wave
- Choices and Challenges
- Technology Evolution
- Value Delivery
- Product Ecosystem
- Development Support
- Indispensability
- Far Reaching Adoption
- Future Ready
- Conclusions
Compute-Intensive Wave
High Performance Computing has Overflowed Original Boundaries

HPC is Increasingly Pervasive

HPC is Increasingly Pervasive

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High Performance Computing has Overflowed Original Boundaries

HPC is Increasingly Pervasive

The Driver?

HPC is Increasingly Pervasive
High Performance Computing has Overflowed Original Boundaries

End User Performance Crave

HPC is Increasingly Pervasive
High Performance Computing has Overflowed Original Boundaries

Why?

HPC is Increasingly Pervasive

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“1 mS of Latency Worth $100M in Stock Trading Business Value”

NYSE Executive - AMD Analysts Day, July 26, 2007
Could it be Worth Less for the Global Airline Reservation System?...
or for Online Business?...

Shopping
Infomedia
Travel
Banking
or for High-Performance Gaming?
We are the Globalized...
Point-and-Click
No Wait =
Zero Latency

Instant Gratification Society

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Creating Strong Demand for High-Performance Compute Infrastructure

Data Centers
Server Farms
Supercomputers
Gaming Platforms
Creating Strong Demand for High-Performance Compute Infrastructure

Data Centers
Server Farms
Supercomputers
Gaming Platforms

The Enabler?
Low-Cost, Off-the-Shelf High-Performance Technology

Interconnects  Multi-Core & Reconfigurable Processors  Virtualization

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Low-Cost, Off-the-Shelf High-Performance Technology

Multi-Core & Reconfigurable Processors

Virtualization

Net Effect?

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Yesterday’s PC Business
Yesterday’s PC Business is Today’s HPC Business
Yesterday’s PC Business is Today’s HPC Business
Carrying Exponential Business Opportunities

HPC Server Revenue by Segments
Source: IDC

<table>
<thead>
<tr>
<th>Price Range</th>
<th>2003</th>
<th>2004</th>
<th>2005</th>
<th>2006</th>
<th>2007</th>
<th>CAQR</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;$95k</td>
<td>1,805,662</td>
<td>2,688,372</td>
<td>2,565,446</td>
<td>2,744,283</td>
<td>2,606,812</td>
<td>10%</td>
</tr>
<tr>
<td>$100K-$249K</td>
<td>946,886</td>
<td>1,116,730</td>
<td>2,561,422</td>
<td>3,323,051</td>
<td>4,193,089</td>
<td>45%</td>
</tr>
<tr>
<td>$250-$499K</td>
<td>543,830</td>
<td>977,380</td>
<td>1,197,234</td>
<td>1,420,357</td>
<td>1,780,539</td>
<td>35%</td>
</tr>
<tr>
<td>&gt;$500K</td>
<td>2,401,478</td>
<td>2,630,877</td>
<td>2,881,105</td>
<td>2,566,886</td>
<td>2,982,811</td>
<td>6%</td>
</tr>
</tbody>
</table>

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Choices and Challenges
The HPC Industry Faces Technology Choices and Challenges
Performance, Scalability are Make-or-Break Factors
Interconnect Technology is Crucial to HPC Product Success

The premium on SYSTEM design continues

- Power
- Reliability / Availability
- Interconnect
- Programmability
  - Debuggability
- Cost:
  - Efficiency vs cost
  - Not Efficiency vs Peak

**NOTE:** Single (or limited) function systems are different
Interconnect Technology is Crucial to HPC Product Success

Future Directions

- Close collaboration on high end systems with partners.
  - Parallelism is available and being exploited. Less emphasis on single thread performance. (It is still very important).
  - Users are accustomed to leveraging “unique” hardware if there is value.
  - Detailed analysis based on real applications.
- Power reduction is achievable.
  - Technology has been “over-leveraged” leaving significant room for power reduction.
  - Power reduction MUST be accompanied by increased capability.
- Node architecture must be accompanied by the overall system architecture.
  - Latency promises to be the biggest challenge for the future of networks.
  - Capability with increased parallelism requires lower latencies.
- Successful direction likely to require frequent introduction of new programming model changes.
  - Some of these are likely to be discarded.
- Exploring the architectural space will require the commitment of industry and government.

“Latency promises to be the biggest challenge for the future of networks”
HyperTransport™
Evolution
That Continues to Evolve
with Expanding Market Presence

2001
HT 1.0

2002
HT 1.1

2004
HT 2.0

2005
HTX™

2006
HT 3.0

2008
HT X3™

Chip-to-Chip

Chip-to-Chip and Beyond

18M HT-Based Systems Shipped
(Note 1)

63M HT-Based Systems Shipped
(Note 2)

Note 1: by end of 2003 – Source InStat
Note 2: by end of 2008 – Source InStat
Adopted by Industry Leaders

in Widest Range of Applications

than any other interconnect technology
HyperTransport™
Value Delivery
HyperTransport Delivers
Key Core Values to HPC Industry

Performance  Scalability  Dependability

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Direct Point-to-Point Link Topology

Performance

CPU-to-CPU-to-Coprocessor

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Direct Point-to-Point Link Topology

CPU-to-High-Performance Subsystems
Direct Point-to-Point Link Topology

CPU-to-I/O Peripherals

Performance
State-of-the-Art Bandwidth

HT 3.1
51.2 GB/s (*)

HT 3.0
41.6 GB/s (*)

2.6 GHz  2.8 GHz  3.0 GHz  3.2 GHz Clock

(*) 32-Bit, Aggregate

4x HT 1.0’s Bandwidth

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Lowest Achievable Latency

No Control Logic Penalty

Control Logic Penalty

Performance

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Lowest Achievable Latency (cont.)

No 8B/10B Overhead Penalty

20% 8B/10B Overhead Penalty vs. HT
Lowest Achievable Latency (cont.)

Performance

Minimized Packet Overhead

Header
8 or 12 Bytes

DATA
4-64 Bytes

Transaction
Data Link Layer
8 or 12 Bytes Overhead

12 Byte Overhead Penalty vs. HT

Sequence Number

Header

DATA
4-4096 Bytes

ECRC

LCRC

Transaction Layer
12 or 16 Bytes Overhead

Data Link Layer
8 Bytes Overhead

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Priority Request Interleaving™

1. Data transfer 1 underway
2. While transfer 1 carries on, PRI occurs
3. Data transfer 2 initiates while data transfer 1 is still underway

Performance

Fastest I/O Interrupt Processing
Predictable Performance Scaling

Clock Forwarding

Synchronous Operation

Scalability

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Asymmetric & Mixed Link Width

2 to 32 Bits per Link

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Architectural Latitude

Asymmetric Link Splitting

Scalability
Asymmetric Link Splitting

1x 4-Bit $\rightarrow$ 2x 2-Bit
1x 8-Bit $\rightarrow$ 2x 4-Bit
1x 16-Bit $\rightarrow$ 2x 8-Bit
1x 32-Bit $\rightarrow$ 2x 16-Bit
Scalability

Link Splitting Flexibility

Fully connected 4-socket node

Fully connected 8-socket node with direct connect between memory controllers

Faster Links, Fewer Hops Better Memory Latency
Architectural Latitude

Scalability

AC Mode

DC Mode

Max Spec at \( \leq 12 \) In

In-System

Decoupling Caps

Max Spec at \( \leq 3 \) Ft

Backplane Chassis-to-Chassis

HT Increasingly Pervasive

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Solution of Choice In Demanding Market Sectors

58 Million
HT-Powered Products
(2007)

<table>
<thead>
<tr>
<th>Capture</th>
<th>Market</th>
<th>Yr/Yr Growth</th>
</tr>
</thead>
<tbody>
<tr>
<td>8%</td>
<td>Defense Applications</td>
<td>17%</td>
</tr>
<tr>
<td>32%</td>
<td>Top500 Supercomputers</td>
<td>28%</td>
</tr>
<tr>
<td>11%</td>
<td>Core Routers</td>
<td>1.2%</td>
</tr>
<tr>
<td>22%</td>
<td>Edge Routers</td>
<td>34%</td>
</tr>
<tr>
<td>15%</td>
<td>SAN</td>
<td>11%</td>
</tr>
<tr>
<td>23%</td>
<td>Servers</td>
<td>38%</td>
</tr>
</tbody>
</table>

Source: InStat

Mature, Stable, Field-Proven Technology

Dependability

Mission-Critical Reliability
Vast HyperTransport™ Product Ecosystem
Fixed Function Control, Bridge ICs

Vast HT Product Ecosystem
FPGA Cores

Vast HT Product Ecosystem

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IP Cores and PHYs

Vast HT Product Ecosystem
Standardized HTX BIOS Support

Embedded into AMI BIOS Code

Aptio

Vast HT Product Ecosystem

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HTX-based Systems and Subsystems

Vast HT Product Ecosystem
FPGA-Based Coprocessors

Vast HT Product Ecosystem

Vacant Opteron Socket

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Testers, Link Analyzers, Verification Tools

Vast HT Product Ecosystem

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HyperTransport™
Development Support
HyperTransport Center of Excellence

Universal HTX Reference Design Boards

HT Cores
Coherent & Non-Coherent

HTX Test Tools

HTX Design & Product Validation Services

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**HTX™ 10GE NIC Design Kit**

Validated and Tested 10GE Solution
Downloadable Free-of-Charge from HTC Web Site

- 2x 10GE Ports
- Stratix II FPGA

Fast Time-to-Market

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HTX™ FPGA Development Board

For Lattice 1.6 Gb/s SC FPGAs
HyperTransport™
Cornerstone of Business Investment
HyperTransport isn’t

A Checkmark on a Features Wish List
HyperTransport is
A Strategic Business Enabler
for
Industry Leaders
Technology Innovators

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“Through 2010, AMD's multi-core processor roadmap and HyperTransport™ technology capabilities stand out for their ability to help meet our aggressive performance goals.”

Peter Ungaro
President and CEO - Cray, Inc.

¾ of Cray’s Product Portfolio
Banking on HyperTransport
Cray XT5h (Hybrid)

“Coupling industry-leading scalar processing capability with high-bandwidth vector processing and reconfigurable FPGA acceleration, the Cray XT5h system establishes a new paradigm in high performance computing.”
Sun Constellation System

Standard Technology-Based Petascale Compute Cluster

"We’re riding the price curve of commodity components, including memory, I/O and CPUs.”

“It enables us to radically reduce the amount of complexity for petascale level clusters, making them easier to deploy and manage, and more efficient to own and operate.”

"Sun is a strong promoter of HyperTransport technology…”
“The AMD Opteron™ processor architecture scales extremely well because of its design that uses integrated memory controllers and fast point-to-point interconnects.”

“Opteron processors use fast, point-to-point HyperTransport links to connect to other processors or I/O. Compared to a shared or bi-directional bus, a point-to-point interconnect has the advantage of no overhead for bus arbitration and easier maintenance of signal integrity.”
“Latency promises to be the biggest challenge for the future of networks.”

LS 21, 41 Blade Servers
System x 3455, 3655, 3755 Servers

HTX™-Equipped
Packet Capture Technology

“Celoxica focuses on addressing some of the most challenging problems facing the finance sector, such as the exponential development of electronic trading and growth of complex derivatives trading, where the company can deliver advantage measured in microseconds.”

Lowest Latency Interface

“HyperTransport is the lowest-latency bus available for communications between peripheral devices and a server's CPU.”
“DRC RPUs provide the most tightly-coupled coprocessing environment possible with direct access to DDR memory and any adjacent Opteron processor at full HyperTransport bandwidth and low latency.”

“The module connects to the CPU's HyperTransport bus and motherboard DIMMs while utilizing the existing power supply and heat sink solution for the CPU.”
Virtualization Processors

“HyperTransport enables the Dynamic Data Center”
HyperTransport™
Far Reaching Adoption
“If the HyperTransport link in the Xbox was a pipe carrying water, and every bit of information equalled one gallon, the pipe would fill up the Pacific Ocean every second!”
NVIDIA Web Site
PowerPC Compute Platforms

Personal Computing & HPC

HyperTransport Consortium Co-Founder

iMac G5

Power Mac G5

Xserve G5
PowerPC Embedded Systems

Embedded Systems

IBM

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Communication Processors

Comm & Networking

HyperTransport Consortium Co-Founders

BCM1125H 64-bit MIPS Processor
BCM 1250 64-bit MIPS Processor
BCM 1280 64-bit MIPS Processor
BCM1480 4-Core 64-bit MIPS Processor

RM9150 64-bit MIPS Processor
RM9200/9100 64-bit MIPS Dual/Single Processor
RM11200 64-bit MIPS Multiprocessor
RM9220/9224 64-bit MIPS Multiprocessor
Knowledge-Based Processors

Real-Time Data Analysis

Tarari T10

Copyright HyperTransport Consortium 2008
Network/Media Processors

Real-Time Data Analysis

Chesapeake

Copyright HyperTransport Consortium 2008
Multi-Threaded Packet Processors

Real-Time Data Analysis

XLR 700 Family
XLR 500 Family
Intel Platforms – Past, Present and Future

General Computing
HyperTransport™
is Everywhere

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Future Ready
Rich HyperTransport™ Technology Pipeline

Extended HT Features

Wider Breadth of Applications

Technical Working Group
Conclusions
With Performance and Scalability
The Make-or-Break Factors...
Can Interconnect Technologies Meet the HPC Challenge?
HyperTransport Can
With Strong Core Values

- Architectural Simplicity
- Protocol Efficiency
- Full Scalability
- Low Design Cost
- Extensive Support
- Vast Product Ecosystem

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With HyperTransport
The Technology Industry Wins

Power
- Highest Bandwidth
- Lowest Latency
- Most Optimized Packet Handling

Tangibility
- Chosen by Industry Leaders
- Massive Market Penetration
- 60M+ HT Systems Shipped

Investment Preservation
- 100% Specs Legacy Compatibility
- Smooth Product Migration
- Future-Ready
Vibrant Technology
Dynamic Consortium

Continue to Lead Industry
and
Deliver State-of-the-Art Value