HTX™ Board
Universal HTX Reference Platform

A Development of the
Computer Architecture Group

UNIVERSITY
OF
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Mannheim, Germany
The HTX Board
Applications

- Rapid Product Prototyping, Time-to-Market
- CPU Processing Off-loading
- Numerical Computing Acceleration
- Server Clustering
- Packet Management
- Network Security Processing
- Media Acceleration
Features

- **Compatible with Any AMD Opteron-based System with HTX Connector**
  - 3.2 GByte/s bandwidth via HyperTransport HTX 400MHz interface
  - Very low latency device access
- **Variety of Standard Interfaces**
- **Programmable Core**
  - Xilinx Virtex-4 FX60 FPGA
  - Platform ROM ensures low configuration time
- **Bidirectional High Speed Serial Links**
  - 6x SFP connectors
  - 1x SATA connector
  - 4x on one SAMTEC high-speed connector
- **DDR2-DRAM (32-bit wide, up to 512 Megabyte)**
- **Flash memory (512 Megabit)**
- **Gigabit-Ethernet Transceiver with RJ45-Connector**
- **Programming Infrastructure via JTAG and USB**
- **Connectors for User-specific Mezzanine Boards**
Block Diagram
HyperTransport / HTX Connector

- **HyperTransport Technology** ([www.hypertransport.org](http://www.hypertransport.org))
  - Processor-native interconnect
  - No intermediate control logic (no latency penalty)
  - No 8B/10B serializing/de-serializing, clock recovery
  - Lean packet protocol
  - Flexible link frequency and width
  - Lowest latency

- **HTX Connector** ([www.hypertransport.org](http://www.hypertransport.org))
  - Standardized specification
  - Available on ever-expanding number of systems/motherboards
  - Commodity connector type (PCIe x1 & x16)
HTX System Implementation
HTX Board - Building Blocks

- **HTX-Board**
  - Available design files: Schematic views, Allegro files, Gerber files, BOM

- **HT-Core**
  - Reference design

- **HTX-Extenders**
  - Flying-Probe based
  - Agilent-specific replacing the probes

- **Mellanox Boards**
  - Debug
  - Two Cat7 connectors

- **In-System Programming using USB**
  - Replacing JTAG parallel programming cable
  - No special hardware for programming required
HTX Board - Sub-modules

- Mezzanine Connectors
- PROM
- GigE
- Flash
- RJ45
- USB-B
- DDR2
- ATOLL compatible links
- HTX connector
- 4x MGT
- One of six SPFs
HTX-Board - Physical Design

- **Hand-Routed, 8-Layer PCB (cost optimized)**
  - 3 power planes (1.2V + 2.5V + splitted)
  - 1 ground plane
  - 4 signal routing layers (2 microstrip and 2 stripline)
  - Stripline-optimized for differential pairs
- **Controlled Impedance**
- **Min. Drill**: 0.2mm
- **Min. Track Spacing/Width**: 75um
- **Number of Connections**: 780
- **Number of Components**: 845
- **Ample Power Distribution Filtering**
  (~500 capacitors)
HyperTransport Core Features

- FPGA Firmware with HyperTransport Management
  - 3,2GByte/s bandwidth via HTX 400 MHz interface
  - Very low latency device access
  - Convenient device interface at end of queues
  - HT interface implemented for Xilinx serializing I/O cells
  - Programmable core logic based on Xilinx Virtex4 FPGA
  - Minimal use of hardware resources
  - Simulation and verification environment
  - Test and debug configuration files for Cadence Simvision
HyperTransport Core
Block Diagram
HyperTransport Core Specifications

- Configurable LVDS Bidirectional Interface (16-bit Wide Max.)
- 200MHz (Max.) Clock for Mapping into Virtex4 FPGA
- Internal Data Path Width of 4x the Link Width (32/64bits)
- Fully Synchronous Design
- Efficient Pipelined Structure
HTX Extender Board
Model A

- For Measurements with Flying Probes
  - Unrestricted usage
  - Testing of complete HTX connector 16-bit interface, power, aux. HTX signals (PWROK, RESET_, JTAG, REFCLK)
HTX Extender Board
Model B

- For Testing with Agilent Logic-State-Analyzers
  - No probes required
  - Same features as HTX Extender Board – Model A
Mezzanine Boards

• Easy Design of Customer-specific Mezzanine Boards (Example: Debug Board)
• Widely Used Samtec Connectors
• I/O Features:
  – 10bit wide LVDS
  – Single-ending possible
• Power Features:
  1.8V and 3.3V
FPGA Programming

- **Traditional Method: via Special JTAG-Cable**
  - Connected to parallel port

- **Improved Method: In-System Programming via USB**
  - USB widely available
  - Connection from Mainboard to HTX-Board via USB-cable
  - No special programming hardware needed
  - JTAG emulated over USB UART device
  - Same functionality as the JTAG-cable
FPGA Programming

Connector

USB Port A

USB Port B

Ethernet
1000/100/10
RJ-45

FLASH
512MBit

Xilinx Virtex4-FX60
BGA1152
576 User I/O
16 MGTs

PPC

PPC

PROM
XCF32P
32MBit

Voltage Supervisor

JTAG chain

4

d_in0
prog b
init b
cclk

4

4

8
SelectMAP

4

4

8

general purpose

manual reset

TDO
TCLK
TMS

computer architecture
Computer Architecture Group
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- Member of HyperTransport Consortium
- Member of Power.org
- Academic Partner of HP

**HTCE - HyperTransport Center of Excellence**
- The HTCE is funded by and works in close cooperation with AMD research facilities in order to improve the HT interface and the IP cores in the scope of the Torrenza initiative.
  - (see also http://htce.uni-hd.de)

**Other Computer Architecture Group’s Projects**
- See http://cag.uni-hd.de
Contacts

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