

**For Immediate Release**



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## **HyperTransport Consortium Extends Signal Transmission Distance by 6x and Provides Flexible Options with New Connector Specifications**

***Enables Full HT3 Bit Rate of 6.4 GT/s and 51.2 GB/s Aggregate Bandwidth Up to 2 Meters***

**SUNNYVALE, Calif., December 10, 2009** –The HyperTransport Consortium today released two new HyperTransport connector/cable specifications that enable more innovative ways of implementing and interconnecting HyperTransport links in data center and high-performance computing platforms. The specifications define a comprehensive portfolio of high-performance, compact and fully standardized connectors and cables capable of carrying HyperTransport links at their full 3.2 GHz clock rate over distances of up to 2 meters with excellent signal integrity, unmatched by traditional printed circuit boards (PCB) technology. The portfolio enables a new breed of board-to-board, system-to-subsystem, system-to-appliance and chassis-to-chassis interconnect solutions for applications such as motherboards, special function subsystems, servers, blade servers and server clusters.

The new specifications standardize a physical layer complement to the High Node Count (HNC) specification released earlier this year by the HyperTransport Consortium. The HNC specification defines extensions to the HyperTransport 3 protocol that answer the industry challenge of addressing the exponentially increasing number of CPU cores and computing nodes in high performance systems.

“We have evolved HyperTransport from the well established role of high performance chip-to-chip interconnect standard, to a full-fledged role of first and only system-wide interconnect standard capable of fulfilling the industry’s most demanding commercial and scientific computing requirements,” said Mario Cavalli, general manager of the HyperTransport Consortium. “Together, the HNC and Connector specifications enable highly scalable, heterogeneous, fully hardware-virtualized and modularized resource-sharing computing platforms that support global shared memory architectures. These are best suited to deliver the performance, energy efficiency and cost optimization that data center and high performance computing markets need going forward.”

The new specifications are the result of collaborative work between the Consortium’s Technical Working Group (TWG) and Samtec, Inc., a world leader in high performance interconnect technology and materials and a member of the HyperTransport Consortium.

“HyperTransport technology delivers leading-edge performance that is the perfect match and proving ground for our interconnect technology expertise,” said David Givens, director of standards and development manager of Samtec, Inc. “Our close cooperation with the HyperTransport Consortium team has enabled us to develop and standardize state-of-the-art interconnect solutions that we expect will open new, enabling opportunities for system design engineers and scalable computing architects.”

The HyperTransport Node Connector Specification defines right angle and vertical mount female cable connectors, as well as a universal male cable connector. The right angle female connector carries 2x independent and stacked 8-bit HyperTransport links in a 30 x 30 x 14.6 mm edge-mount shell for motherboard and add-on cards use. The vertical mount female connector is a 27 x 9 x 8.7 mm small footprint connector that can easily be positioned anywhere on system motherboards or add-on cards and it allows a system’s CPU to be directly linked to either in-chassis or external HyperTransport subsystems. Both the right angle and vertical mount female connectors are compatible with the 27 x 25.4 x 6.1 mm universal male cable connector. Either 8-bit link or 16-bit HyperTransport link configurations are supported.

The HyperTransport Mezzanine Connector Specification defines highly compact, vertical mount male and female connectors measuring 55.7 x 8.3 x 10.6 mm and 56.6 x 5.6 x 5 mm respectively and supporting 2x 8-bit or 1x 16-bit HT link configurations and which can be used for stacked, board-to-board connections without the use of cables. The mezzanine connectors carry a number of user definable pins are ideally suited for in-system, add-on function modularity in the form of multi-processor modules, network interface cards, acceleration modules and any special function modules.

The mechanical structure and the signal, ground and power pins allocation of all standardized HyperTransport connectors have been defined to produce the best escape routing PCB designs.

### **About the HyperTransport™ Technology Consortium**

The HyperTransport Technology Consortium is a membership-based, non-profit organization that licenses, manages and promotes HyperTransport Technology. The HyperTransport Consortium was founded in 2001 by leading technology innovators like AMD, Broadcom, Cisco, NVIDIA and Sun Microsystems and counts several industry-leading members worldwide, including AMD, Broadcom, Cisco, Cray, Dell, HP, IBM, NVIDIA and Sun Microsystems. Consortium membership is based on a yearly fee and it is open to companies interested in licensing the royalty-free use of HyperTransport technology and intellectual property. Consortium members have full access to the HyperTransport technical support database, they may attend Consortium meetings and events and may benefit from a variety of technical and business promotion services that HTC offers at no cost to its members.

To learn more about member benefits and how to become a Consortium member, please visit the Consortium Web site at <http://www.hypertransport.org>.

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