For Immediate Release

Press Contact:
Erika Powelson
Tanis Communications
831-424-1811
email: erika@taniscomm.com

Reader Contact:
Mario Cavalli
HyperTransport Consortium
925-968-0220
email: mario.cavalli@hypertransport.org

HyperTransport Consortium Maintains Interconnect Performance Leadership with New 3.0 Specification

41.6 GB/s Aggregate Bandwidth, New Features Extend Signal Distance To Enable Expansion Into Chassis-to-Chassis and Board-to-Board Interconnect Applications

Sunnyvale, Calif., April 24, 2006 -- HyperTransport™ Technology Consortium, a standards organization dedicated to developing the industry's lowest latency, highest bandwidth interconnect technology, today released version 3.0 of the HyperTransport specification. The new standard nearly doubles the bandwidth and speed of the previous HyperTransport 2.0 specification. In addition, HyperTransport 3.0 supports a variety of new features including AC coupling mode, hot plugging, un-ganging mode and dynamic power management for the support of extended signal transmission distance, typical of backplane and chassis-to-chassis implementations. HyperTransport 3.0 builds on the existing HyperTransport 1.0 and 2.0 standards which continue to be designed into end systems at an accelerating rate, and have helped HyperTransport reach considerable market presence and success. HyperTransport 3.0 is fully backwards-compatible with earlier versions of the HyperTransport specification standard.

"The added performance and new features of HyperTransport 3.0 extend the applicability of HyperTransport technology from chip-to-chip and board-to-board, all the way to chassis-to-chassis applications," said Mario Cavalli, general manager of the HyperTransport Technology Consortium. "HyperTransport has proven to be the industry's most flexible, powerful and future-ready standard interconnect solution for compute-intensive system designs, delivering a winning combination of high-performance, standardization and optimized total cost of ownership (TCO) for data center and supercomputing applications."

There are over 40 million[1] HyperTransport technology-enabled systems in perhaps the industry's widest range of applications for interconnect technologies. HyperTransport technology is deployed in applications ranging from high-performance embedded systems to personal computing, workstations, servers, supercomputers and clusters.

[1] Source In-Stat, "I/O, I/O How Much Faster Can We Go: Chip-to-Chip Interconnects," October 2005.

HyperTransport 3.0 extends the 1.4 GHz dual data rate (DDR) maximum clock of HyperTransport 2.0 to 1.8 GHz, 2.0 GHz, 2.4 GHz and 2.6 GHz, and delivers a maximum aggregate bandwidth of 41.6 gigabytes per second (GB/s) - a bandwidth increase of 86 percent over HyperTransport 2.0.

"As processor performance continues to rise, and the industry increasingly moves toward a new generation of multi-core technology, multi-CPU system designs, interconnect latency and bandwidth take on a pivotal role in overall system and application performance," said David Rich, president of the HyperTransport Consortium. "By further reinforcing HyperTransport's industry position as the lowest latency, highest bandwidth interconnect technology, HyperTransport 3.0 enables designers to achieve state-of-the-art application performance and optimum time-to-market advantages while benefiting from the combined economies of scale of a widely adopted interconnect standard and a full array of off-the-shelf systems and components."

Technical Features and Benefits of HyperTransport 3.0

- **AC mode (Optional)** – An innovative AC interconnect mode complements HyperTransport's traditional DC mode, featuring capacitor coupling, AC/DC auto-sensing and auto-configuring capabilities. The feature extends HyperTransport's maximum signal transmission distance to 1 meter at maximum specified clock speed with no signal transmission or performance degradation. As a result, the HyperTransport standard can now support long-haul signal transmission typical of backplane and chassis-to-chassis applications. During power-up and in total transparency to system software, HyperTransport 3.0 auto-senses the presence of coupling capacitors (AC) and/or direct connections (DC) within the HyperTransport interconnect fabric and automatically configures each portion of it accordingly.
- **Hot plugging** – HyperTransport technology-enabled devices can be added to or removed from the HyperTransport fabric without disrupting system operations. HyperTransport cards, systems and subsystems can therefore be deployed in backplane and any mission-critical platforms requiring high system availability.
- **Un-ganging mode (Optional) –** During system power-up and transparently to system software, 1x16 HyperTransport links can optionally be configured as 2x8 virtual links. This gives system architects extended interconnect flexibility and the ability to fully leverage existing HyperTransport components and cores. Un-ganging mode is particularly valuable in multiprocessor and symmetric multiprocessing environments.
- **Power Management Mode –** HyperTransport 3.0 carries dynamic, auto-sensing, hardware-based, self-configuring power management capabilities that give end products the intelligence to best optimize the power consumption of each of their HyperTransport components and modules in real-time and transparently to operating system (OS) and application software.

Member Companies Support HyperTransport 3.0

"Today's announcement is not only a celebration of HyperTransport technology's increasing adoption across a broad spectrum of commercial and consumer markets, but also enables AMD to continue to expand it's position as an industry leader," said Randy Allen, Corporate Vice President, Server and Workstation Division, AMD. "When AMD originally developed HyperTransport technology, it was with the goal of enabling the most scalable, high performance systems for enterprise computing. The flexibility and scalability that HyperTransport provides not only allows AMD to provide the best performing solutions in the industry, but when combined with inherently power-efficient processor architectures, such as the AMD Opteron(TM) processor, allows for industry leading performance per Watt, as well."

"Cray has a long-standing history of designing and delivering supercomputers with superior interconnects," said Steve Scott, Chief Technology Officer of Cray Inc. "HyperTransport technology provides an ultra low latency, high bandwidth connection directly from the processor's memory system to our high speed network. We've integrated it into two of our current product lines, the Cray XT3 and Cray XD1 systems. Together with our strategic partner, AMD, we expect to continue this practice in future product generations."

“As a leading supplier of current generation HyperTransport link layer cores, GDA Technologies is committed to helping its customers in computing and networking markets adopt the latest in high speed interconnect technology,” said AG Karunakaran "AGK", president of GDA Technologies, Inc. “We are proud to be one of the first IP and service providers to provide synthesizable link layer cores utilizing the new HyperTransport 3.0 and providing support for different HyperTransport configurations.”

About HyperTransport™ Technology and the HTX™ Connector

HyperTransport is the industry's lowest latency, highest-performance, fully scalable, packet-based interconnect technology serving a wide range of industry segments. It is based on two 2-line to 32-line, asymmetric Low Voltage Differential Signaling (LVDS) links, delivering up to 41.6 GB/s of aggregate CPU to CPU, CPU to I/O bandwidth in a highly efficient point-to-point, daisy-chain topology that replaces complex multi-level, multi-line buses and extends from chip-to-chip to chassis-to-chassis applications.

The HyperTransport Consortium has also released the HyperTransport HTX™ connector specification which enables system designers to link high-performance peripheral subsystems directly to the system’s CPU or CPUs via low-latency HyperTransport links. The HyperTransport HTX™ connector makes compute intensive, leading edge CPU-to-I/O and board-to-board designs a reality for a full range of new-generation high performance peripheral functions, such as server clustering, network security, real-time data analysis and routing, storage management, math algorithms acceleration, encryption/decryption, advanced 3D rendering and live video processing, medical imaging and other compute-intensive co-processing functions.

HyperTransport technology is natively embedded in multiple CPU families from AMD, Broadcom, IBM, NetLogic Microsystems, PMC-Sierra, Raza Microelectronics and Transmeta and in a variety of semiconductors and IP cores. It is fully software-compatible with legacy Peripheral Component Interconnect (PCI), PCI-X and PCI Express technologies.

HyperTransport technology-enabled devices are deployed in high-profile products in networking, consumer, personal computers, workstations, servers and supercomputers from a wide range of companies including Apple, Cisco, Cray, Hewlett Packard, Fujitsu-Siemens, IBM, Lenovo, Microsoft, Sharp, Sun, and all PCs, servers & cluster workstations based on AMD Sempron™, AMD Athlon™ 64 and AMD Opteron™ processors, as well as AMD Turion™ 64 Mobile Technology and Transmeta Efficeon processors.

About the HyperTransport™ Technology Consortium

The HyperTransport Technology Consortium is a membership-based, non-profit organization that manages, promotes and licenses HyperTransport Technology. The HyperTransport Consortium consists of over 40 industry-leading member companies, including founding member Advanced Micro Devices, Alliance Semiconductor, Apple, Broadcom, Cisco Systems, NVIDIA, PMC-Sierra, Sun Microsystems and Transmeta. Membership is based on a yearly fee and it is open to any company interested in licensing the royalty-free use of HyperTransport technology and intellectual

property. Consortium members have full access to HyperTransport technical documents database, they may attend Consortium meetings and events and may benefit from a variety of technical and marketing services, including the new, member-driven web portal, whose business benefits are part of a wide array of services offered by the Consortium free of charge to member companies. To learn more about member benefits and on how to become a Consortium member, please visit the Consortium Web site at www.hypertransport.org/consortium/cons_join.cfm. Specifications, overviews and white papers about HyperTransport technology can be found at www.hypertransport.org/tech/index.cfm.

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